



PDTA123YQB

50 V, 100 mA PNP resistor-equipped transistor;

R1 = 2.2 k Ω , R2: 10 k Ω

24 November 2023

Product data sheet

1. General description

100 mA PNP Resistor-Equipped Transistor (RET) in an ultra small DFN1110D-3 (SOT8015) leadless Surface-Mounted Device (SMD) plastic package with side-wettable flanks.

NPN complement: PDTC123YQB

2. Features and benefits

- 100 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint

3. Applications

- Digital applications
- Cost saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

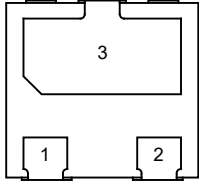
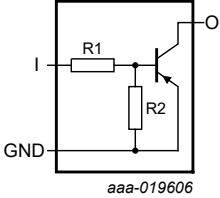
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current		-	-	-100	mA
R1	bias resistor 1 (input)	[1]	1.54	2.2	2.86	k Ω
R2/R1	bias resistor ratio	[1]	3.6	4.5	5.5	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 100 mA PNP resistor-equipped transistor; R1 = 2.2 k Ω , R2: 10 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p>Transparent top view DFN1110D-3 (SOT8015)</p>	 <p>aaa-019606</p>
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA123YQB	DFN1110D-3	plastic, leadless extremely thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.65 mm pitch; 1.1 mm x 1 mm x 0.48 mm body	SOT8015

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTA123YQB	QD

8. Limiting values

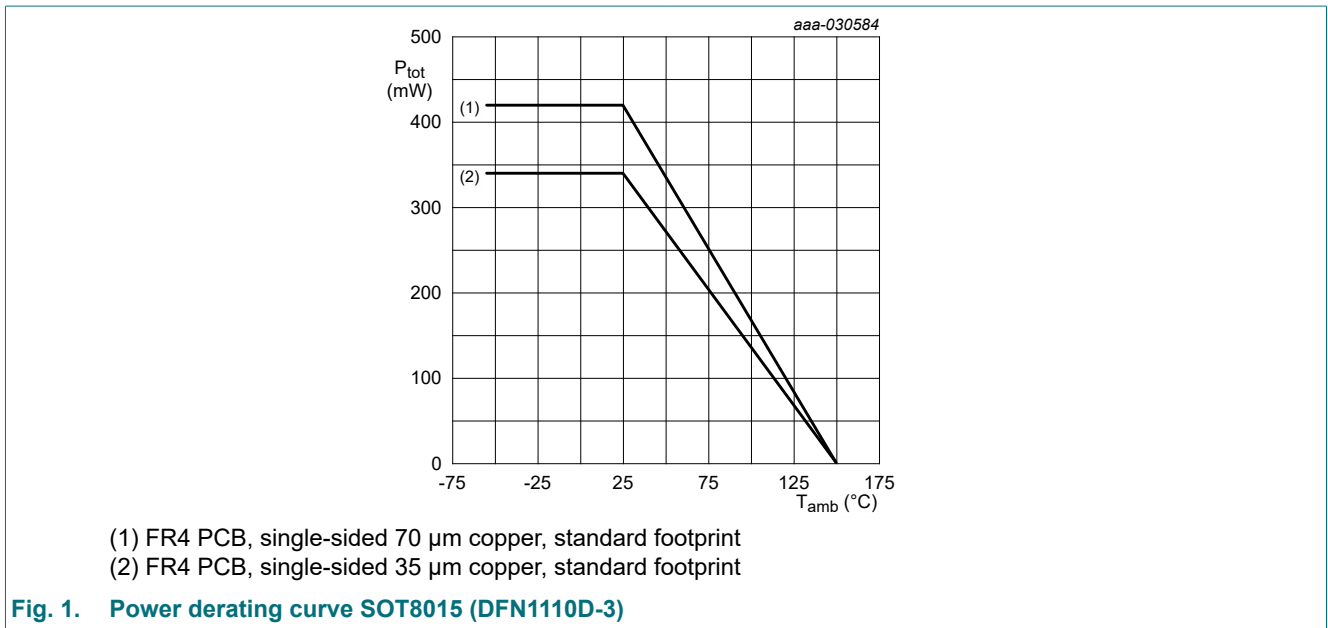
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{CBO}	collector-base voltage	open emitter	-	-50	V	
V_{CEO}	collector-emitter voltage	open base	-	-50	V	
V_{EBO}	emitter-base voltage	open collector	-	-5	V	
V_I	input voltage		-12	5	V	
I_O	output current		-	-100	mA	
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	340	mW
			[2]	-	420	mW
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-55	150	°C	
T_{stg}	storage temperature		-65	150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB; single-sided; 70 μm copper; tin-plated and standard footprint.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	368	K/W
			[2]	-	-	298	K/W

- [1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB; single-sided; 70 μm copper; tin-plated and standard footprint.

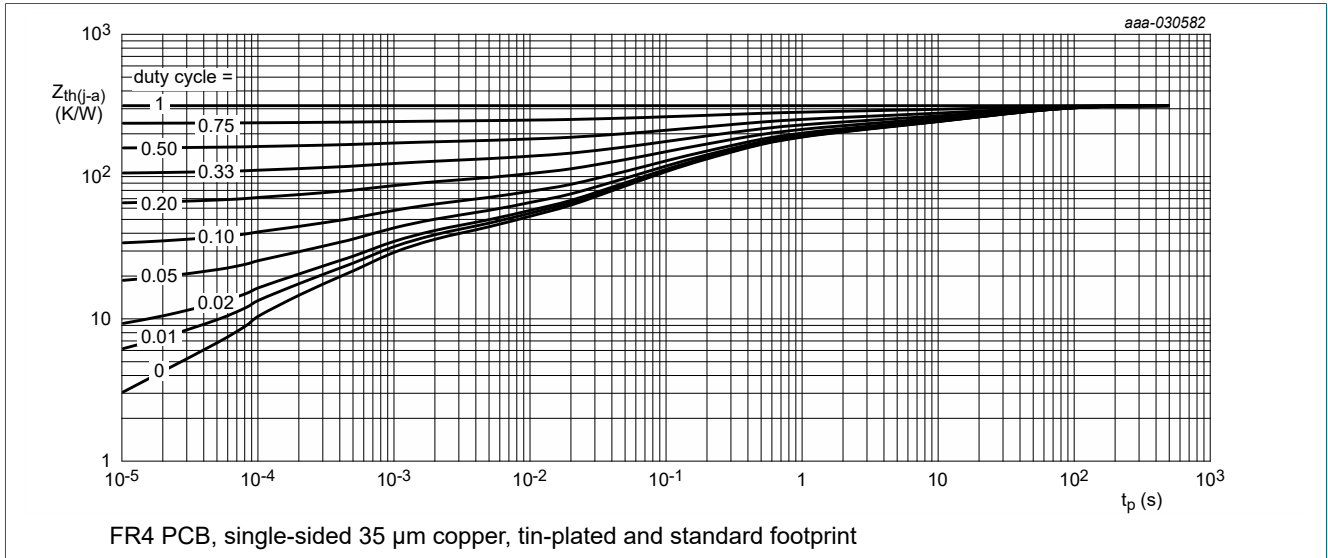


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

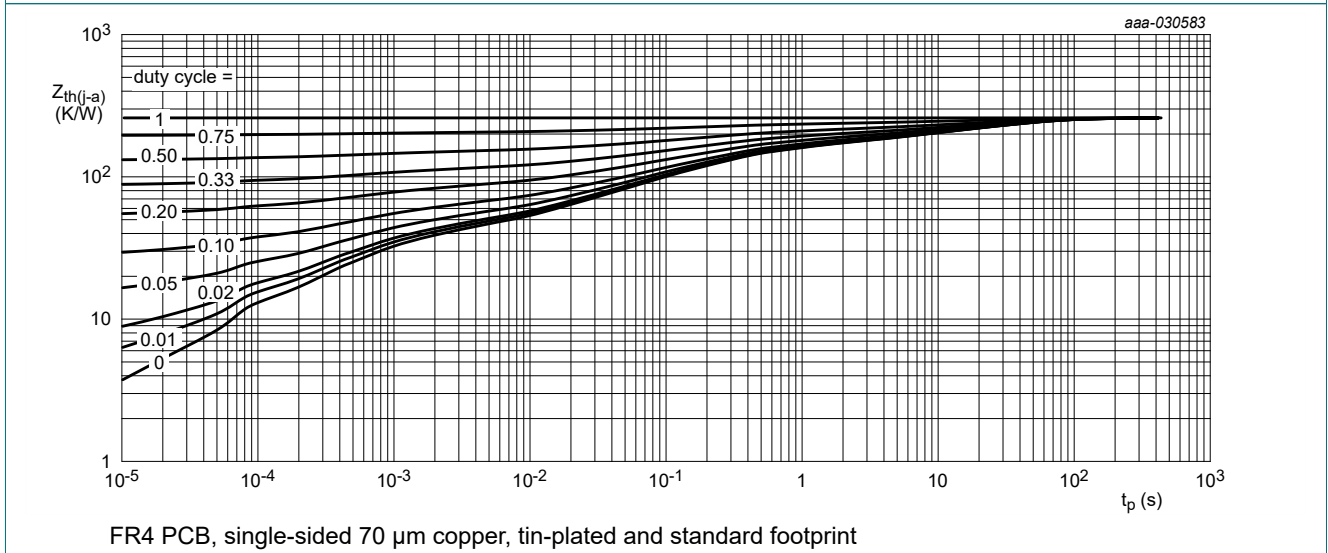


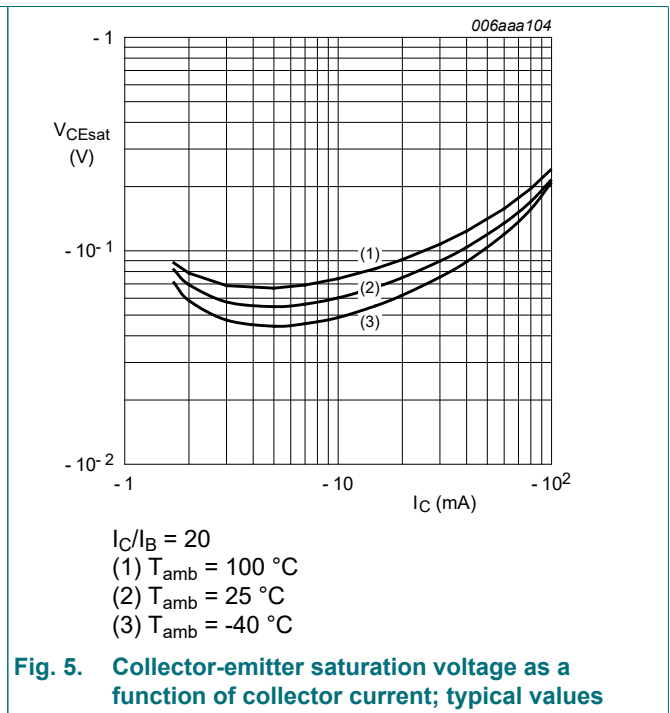
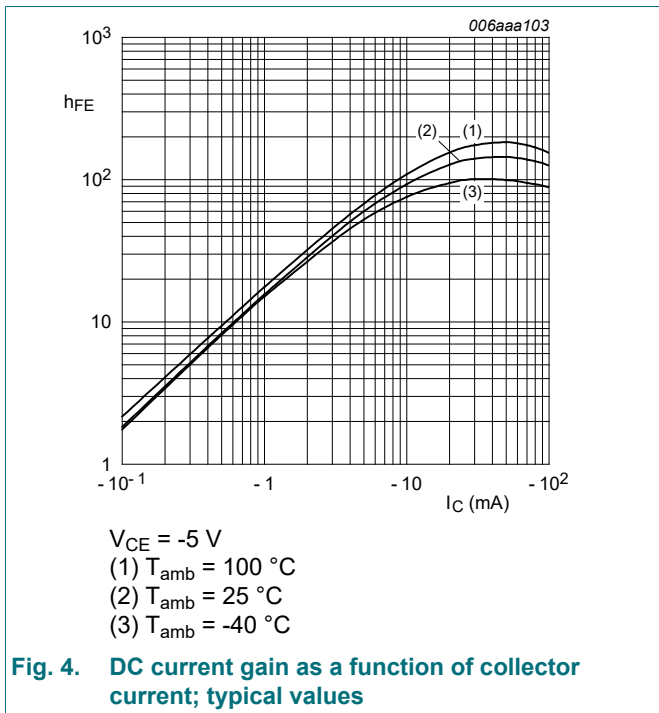
Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu A; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 \text{ mA}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
I_{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	-100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	-100	nA	
		$V_{CE} = -30 \text{ V}; I_B = 0 A; T_j = 150 \text{ }^\circ C$	-	-	-5	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	-700	μA	
h_{FE}	DC current gain	$V_{CE} = -5 \text{ V}; I_C = -5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	35	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	-	-	-150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}; I_C = -100 \mu A; T_{amb} = 25 \text{ }^\circ C$	-	-0.75	-0.3	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -300 \text{ mV}; I_C = -20 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	-2.5	-1.15	-	V	
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	3.6	4.5	5.5	
C_c	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	-	-	3	pF	
f_T	transition frequency	$V_{CE} = -5 \text{ V}; I_C = -10 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	[2]	-	180	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.



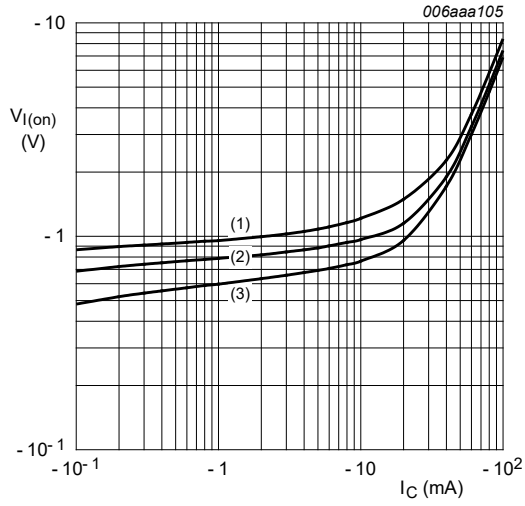


Fig. 6. On-state input voltage as a function of collector current; typical values

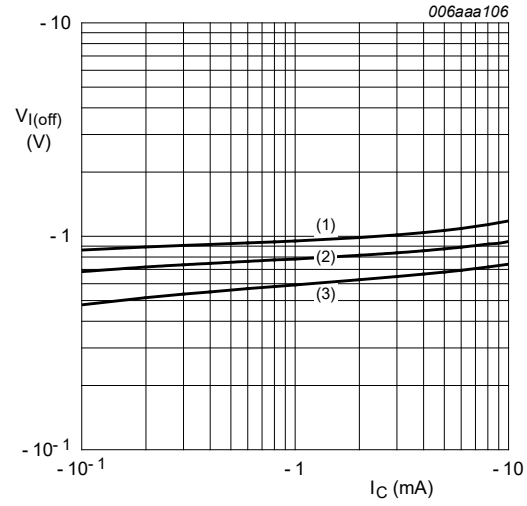


Fig. 7. Off-state input voltage as a function of collector current; typical values

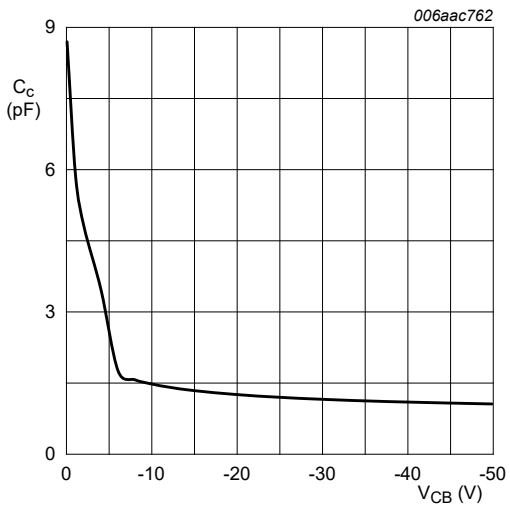


Fig. 8. Collector capacitance as a function of collector-base voltage; typical values

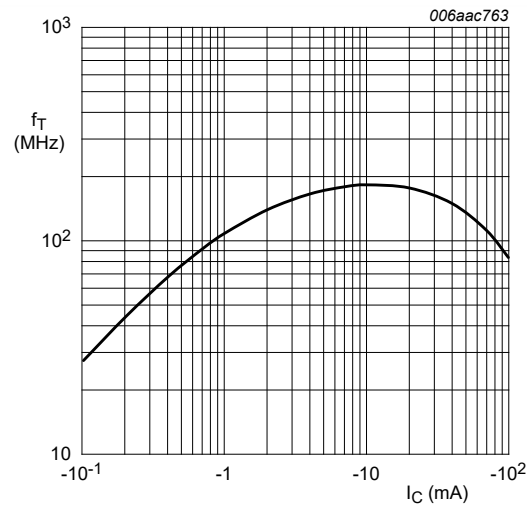


Fig. 9. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

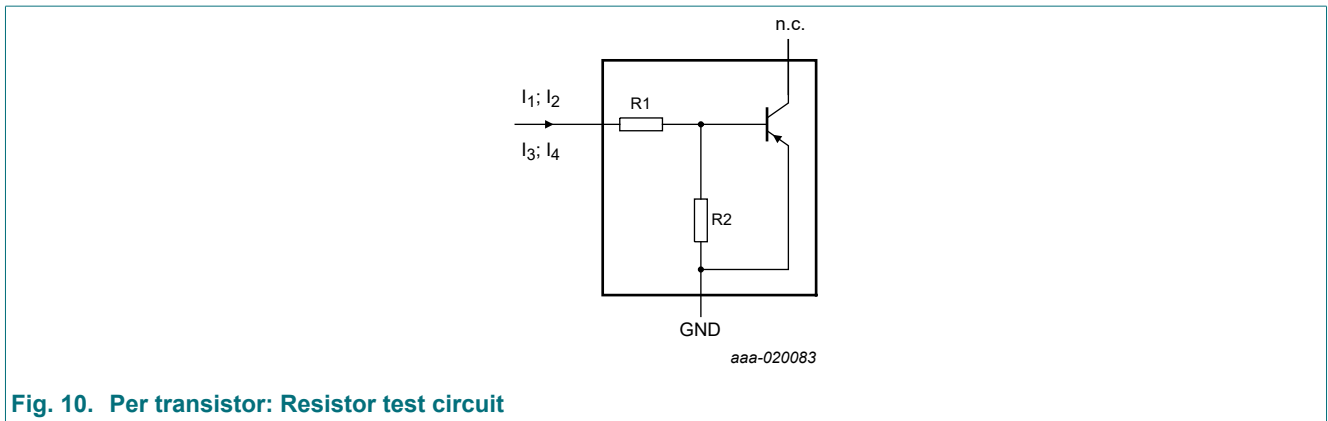


Fig. 10. Per transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PDTA123YQB	2.2	10	-1300 μA	-1500 μA	350 μA	450 μA

12. Package outline

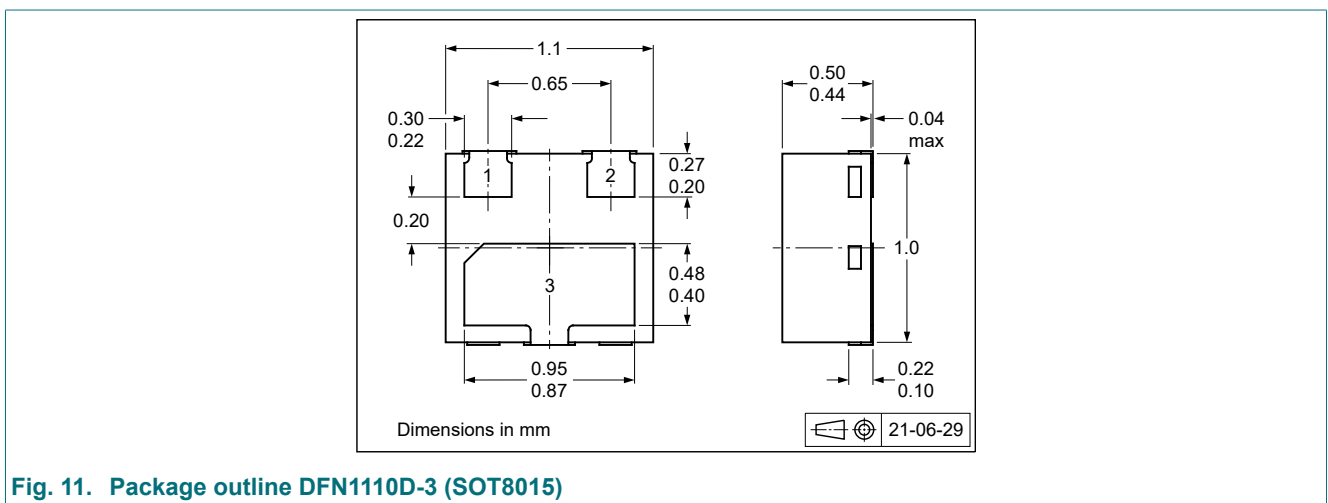


Fig. 11. Package outline DFN1110D-3 (SOT8015)

13. Soldering

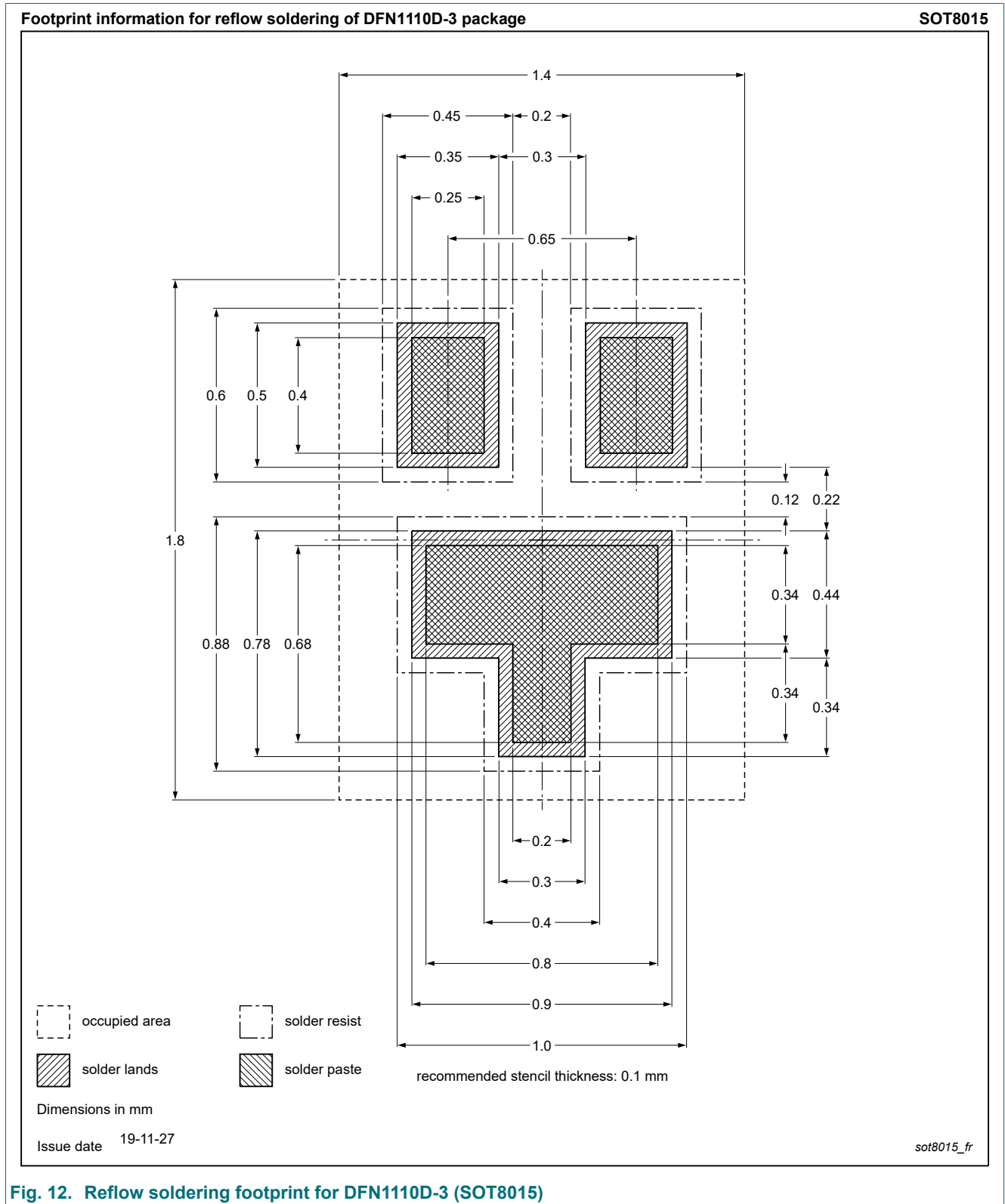


Fig. 12. Reflow soldering footprint for DFN1110D-3 (SOT8015)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA123YQB v.1	20231124	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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